Design of a Novel Dual-core Ultrasonic Nondestructive Testing System Based on ARM and FPGA

Chao Peng[1*], Weiheng He[1], Yue Song[1], Sha Zou[2]

[1]School of Electrical Engineering and Intelligentization, Dongguan University of Technology, Dongguan, 523808, China

[2]HengNan County Seventh Middle School, Hengyang, 421000, China

*E-mail: pengchao@dgut.edu.cn

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Abstract: In this paper, a new system for nondestructive testing in the field of ultrasonic nonmetal detection is designed. The paper first analyzes the design difficulties and technical challenges in the ultrasonic nondestructive testing system. Then the complementarity between ARM and FPGA is used to design a complete set of ultrasonic non-destructive testing system with dual core as the main control. The system mainly includes ultra low noise variable gain amplifier module VGA, anti-aliasing filter module, high speed digital-to-analog converter module ADC, precision gain control DAC, precision voltage source and clock source module and ARM+FPGA master module. Finally, the correctness and rationality of the design are verified by establishing the circuit model of digital signal processing and the actual circuit. The dual-core ultrasonic nondestructive testing system designed in this paper not only has good expansibility, is easy to use in the field, but also has smaller size and lower power consumption. At the same time, it can further reduce the hardware cost of the ultrasonic imaging system, and also lay a solid foundation for other ultrasonic testing systems and equipment, and has good engineering application value.

1. Introduction

Ultrasound is a kind of sound wave whose frequency is higher than 20,000 Hz. It has the characteristics of good direction, high power, strong penetration, easy to obtain concentrated sound energy, and no damage to the detected substances and human body.These advantages make ultrasound widely used in medical[1, 2], military[3, 4], agricultural and almost all industrial flaw detection fields[5, 6]. In addition, ultrasonic detection has a lot of in-depth research and application in thickness measurement[7, 8], ranging and medical ultrasound imaging[9, 10].Nondestructive testing (NDT) is a frequently used analytical tool in scientific research and industry to evaluate the properties of materials and components without damaging or permanently changing them. This can save a lot of money and time, so it is widely used in machine engineering, electrical engineering and civil engineering in many areas of product evaluation, fault detection and research[11-13].At the same time, with the development of integrated circuits and digital signal processing algorithms, the requirements for the performance and diagnostic capabilities of ultrasonic non-destructive testing in the industrial and medical fields are also increasing.

The design of modern ultrasonic nondestructive testing systems has the following difficulties and technical challenges:

(1) Conventional ultrasound imaging systems require a large number of high performance transmitters and receivers, resulting in a large and expensive system. With the development of integrated circuits, we also need to reduce the size and power consumption of written ultrasonic non-destructive testing instruments, thereby extending battery life and simplifying field use.

(2) As devices become smaller, especially with the goal of improving image quality, heat dissipation becomes very important.

(3) In order to improve the signal penetration rate and harmonic imaging, a higher transmission voltage is needed

2. Overall design of twin-core ultrasonic nondestructive testing system

After analyzing the difficulties and challenges of ultrasonic non-destructive testing system design, we designed the overall block diagram of the system using ARM+FPGA dual-core master control mode, as shown in Figure 1. The system includes ultra low noise variable gain amplifier module VGA, anti-aliasing filter module, high speed digital-to-analog converter module ADC, precision gain control module DAC, precision voltage source and clock source module, ARM+FPGA master module and transmit circuit driver modules etc.

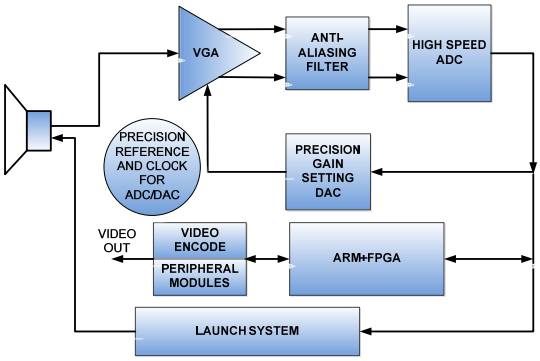

Figure 1 Overall Block Diagram of System

The transmitting circuit driving module can use the conventional capacitor instantaneous discharge method to generate high voltage pulses, or can be realized by a combination of a new high speed waveform generator and a high voltage operational amplifier. Anti-aliasing noise filters are often used in conjunction with ADCs. The filter requirements depend on the application. When the ADC is on another board, most of the filter components should be placed nearby to suppress noise between the boards and to reduce the charge backlash at the ADC input.

3. Design of VGA Module

As shown in Figure 2, we use AD8334 to construct VGA module. AD8334 has four channels, ultra-low noise, linear dB, pre-amplifier and programmable input resistance.When the gain slope control pin MODE goes high (if available), the gain slope is negative. The pin is set to HI gain mode to select the reverse gain mode. It is from −4.5dB to +43.5dB in LO gain mode and +7.5 dB to +55.5 dB in HI gain mode. The LNA intermediate power supply bypass pin LMD must be bypassed to ground and the signal is supplied to the INH pin for capacitive coupling with a 2.2nF to 0.1μF capacitor. The LNA's unterminated input impedance is 6kΩ, allowing users to synthesize any LNA input resistor from 50Ω to 6kΩ.The common-mode voltage-AC bypass pin VCM is typically set to 2.5V. A 1nF capacitor should be placed in parallel with a 0.1μF capacitor and the 1nF capacitor should be placed as close as possible to the VCM pin. The gain control voltage GAIN recommends using a bypass capacitor of 100pF to 1nF.The output clamp level pin RCLMP provides the user with a way to limit the output voltage swing.

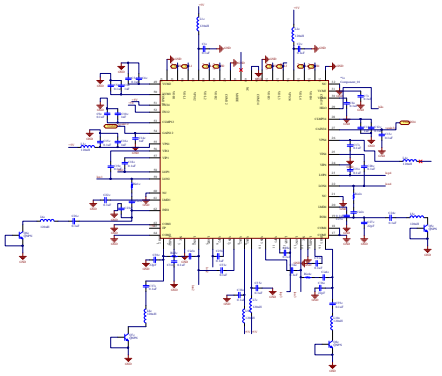

Figure 2 VGA Module Schematic Diagram

4. Design of Precision Gain Control Module

The AD5686R is used to achieve precise gain control. The specific design is shown in Figure 3.

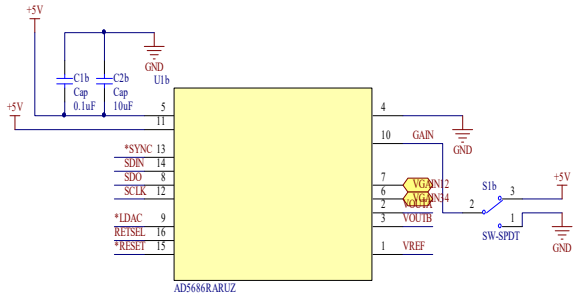

Figure 3 Precision Gain Control Module Schematic

The AD5686R is controlled by the FPGA, and then the control signal is transmitted to the VGA through digital-to-analog conversion to control its gain.The power supply VDD is decoupled to GND through a parallel 10μF capacitor and a 0.1μF capacitor. The power supply VLOGIC is powered by a +5V digital power supply.AD5686R data frame synchronization signal pin SYNC, serial data input SDIN, serial data output SDO, serial clock input SCLK, *LDAC, power-on reset pin RESTSEL, asynchronous reset input pin *RESET are all connected to the FPGA through the SPI bus, and the input and synchronization are controlled by the FPGA.AD5686R's controllable gain pin GAIN can control two-stage gain either at ground level or at high level. When this pin is connected to GND, the output range of all four DACs is 0V to VREF. If this pin is tied to VDD, the output range of all four DACs is 0V to 2 × VREF (VREF is the chip's own reference voltage, the value is 2.5V).The output pins of the chip, OUTA, VOUTB, VOUTC, and VOUTD, are the analog output voltages of the DAC and are connected to the corresponding ports of the VGA.

5. Design of High Speed Digital to Analog Conversion Module

The AD9257 is an 8-channel, 14-bit, 40/65 MSPS serial low voltage differential signaling (LVDS) analog-to-digital converter. The specific design is shown in Figure 4.

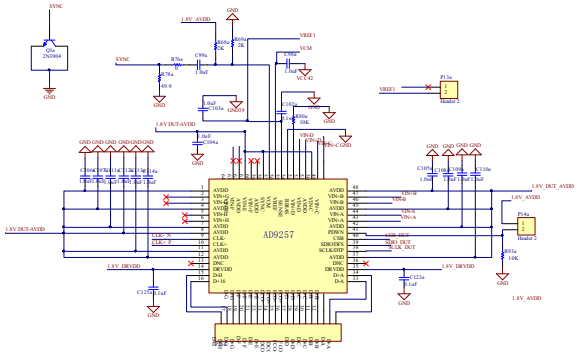

Figure 4 AD9257 Main Schematic

The AD9257 is available in an LFCSP package with an exposed pad on the bottom that requires adequate grounding for proper operation. It is connected to the analog ground through a square of multiple vias to help dissipate heat. The VCM pin should be decoupled to ground with a 0.1μF capacitor. All power supply pin inputs on the chip require a 0.1uF high frequency filter capacitor. The capacitor should be as close as possible to the power supply pin of the chip. The SPI port should be disabled when the converter is required to take full advantage of its full dynamic performance.

5.1. Design of analog input terminal for AD9257

The analog input of AD9257 is a differential switched capacitor circuit, which leads to its suitability for processing the differential signal converted from the single input signal of AD8334.

In order to reduce the high differential capacitance of the input and achieve the maximum bandwidth of ADC, low Q inductance or ferrite beads must be used to drive the front end of the converter at high and medium frequencies. Here we use differential transformer coupling drive ADC input mode. As shown in Figure 5.

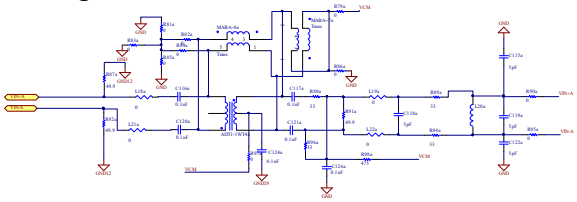

Figure 5 Analog Input Schematic of AD9257

ADT1-1WT RF transformer is used to achieve input-output impedance matching, DC isolation, common-state suppression and balance transformation. The turn ratio is 1:1. Because the transformer is passive, it will not amplify the signal noise. The transformer without gain makes the signal ripple and roll-off more significant. The differential signal input on the left side has 0.1uF capacitor to isolate DC. The design of input impedance and output impedance is close to 50 ohms, so impedance matching can be achieved. The output terminal of transformer is also separated by 0.1uF capacitor. The differential signal indirect 5pF capacitor can suppress the differential mode interference. The effect of MABA007159-000000 transformer is similar to that of ADT1-1WT. Dual transformer topology can achieve better performance in analog input, but PCB layout plays an important role. When adding this transformer layout, it should be symmetrical as possible, otherwise the use of dual transformer topology will not work.

5.2. Design of AD9257 Power Supply Module

In order for the high speed analog-to-digital converter to perform at its best, it must be supplied with a clean DC power supply. High noise power supplies can cause signal-to-noise ratio (SNR) drops and/or undesirable spurious components in the ADC output. In this system we use the ADP1706, which operates from a 2.5V to 5.5V supply with a maximum output current of 1A. At the same time, the system also uses the DC-DC converter ADP2108 to provide 1.8V digital power and 1.8V analog power to the system. The ADP2108 is a high efficiency, low quiescent current, step-down DC-DC converter with excellent stability and transient response. The specific design is shown in Figure 6.

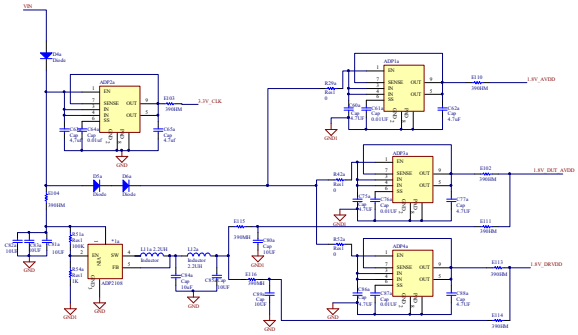

Figure 6 Schematic Diagram of AD9257 Power Module

The 4.7uF capacitor beside ADP1706 can achieve excellent transient response performance of line and load, while the decoupling capacitor of 0.1uF can reduce the fluctuation of power supply voltage. When using the DC-DC converter chip ADP2108, the EN can be connected to 100K and 1K resistor voltage divider first, and the EN level can be lowered. The conversion from ADP2108 to 1.8V_AVDD and 1.8V_DRVDD can be temporarily disabled.The front end of ADP2108 uses three 10uF capacitors to filter the DC input power supply, providing a stable voltage value for ADP2108. The output terminal of ADP2108 is connected with a second-order filter circuit to enhance the filtering of DC voltage and obtain a stable output voltage. In the power supply system, a number of 39 Euros magnetic beads are used to suppress high frequency noise and peak interference, and also

to absorb electrostatic pulses. The magnetic beads have high resistivity and permeability, which are equivalent to series resistance and inductance. All output voltages are decoupled by parallel connection of multiple 0.1uF and 10uF capacitors to reduce the fluctuation of power supply voltage.

5.3. Design of AD9257 Clock Module

Considering the cost and complexity of implementation, the system adopts Silabs Si530 clock chip, which has excellent jitter performance. The typical value of phase jitter is 0.36 PS in the output frequency range of 125 Hz to 500MHz. Unlike traditional clock chip, its built-in fixed frequency can support arbitrary frequency output from 10 MHz to 945 MHz, and support three levels of LVDS, CMOS and LVPECL. To take full advantage of the performance of the AD9257, the Si530 differential LVDS output clock signal is ac-coupled to the AD9257 sample clock terminals (CLK+ and CLK-). The circuit design is shown in Figure 7.

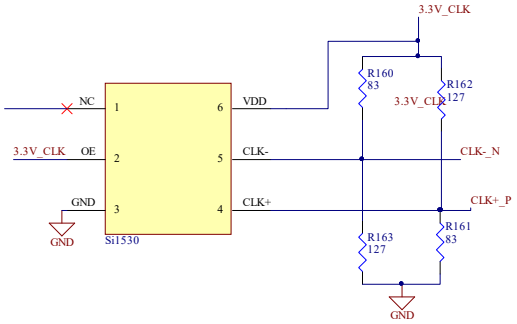

Figure 7 Schematic Diagram of the AD9257 Clock Module

GND is analogically isolated from digital signals, OE pins are enabling pins, VDD pins are power supply pins, all use 3.3V_CLK, while R160, R161, R162 and R163 provide bias voltage to differential clock signals, which enhances the ability of low jitter. High-speed and high-resolution ADC is very sensitive to the quality of clock input signal. When designing the clock of ADC, the problem of aperture jitter should be carefully considered. In order to reduce the influence of aperture jitter on AD9257, the clock input signal is regarded as an analog signal, and the clock drive power supply is isolated from the ADC output driver power supply to avoid the clock signal mixed with digital noise.

5.4. Design of AD9257 Serial Port Function

The AD9257 serial interface (SPI) allows the user to configure the converter with a structured register space inside the ADC to meet specific functional and operational needs. SPI is flexible and can be tailored to specific applications. When the ADC needs to take full advantage of its dynamic performance, to disable the SPI port, usually the SLCK signal, CSB signal, SDIO signal and ADC clock are asynchronous, the noise in these three signals will reduce the conversion performance of the ADC, if other devices use the board When the SPI bus is on, it is recommended that the bus be connected to the AD9257 via the buffer NC7WZ16P6X to prevent these signals from changing during critical sampling periods. The specific design is shown in Figure 8.

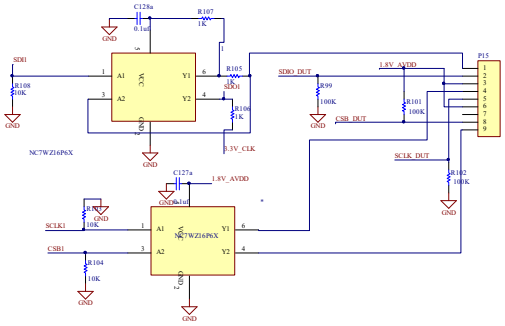

Figure 8 AD9257 Serial Port Schematic

6. Physical Production and Testing

After theoretically designing the circuit, we use PROTEL to simulate the entire circuit design into a compact printed circuit board, as shown in Figure 9.PCB uses four layers, the top and bottom layers are signal wiring layers, and the middle two layers are negative layers as strata and power layers. The strata are divided into AGND (analog ground) and DGND (digital ground). AGND and DGND are connected by ferrite beads or 0_resistance.The power layer is divided into + 5V, 1.8V_DUT_AVDD analog power supply for ADC, 1.8V_DRVDD for ADC digital output power supply, and 3.3V_CLK for clock power supply. The design rules are that the ground wire is wider than the power line, the power line is wider than the signal line, and different power sources should ensure that there is no interference between them. The signal line should be as far away as possible from the power signal line, the analog power supply and the digital power supply should be isolated from each other, and the ground wire should be as short and thick as possible to avoid large voltage drop between the ground lines. Subsequently, it is made into physical objects, as shown in Figure 10.

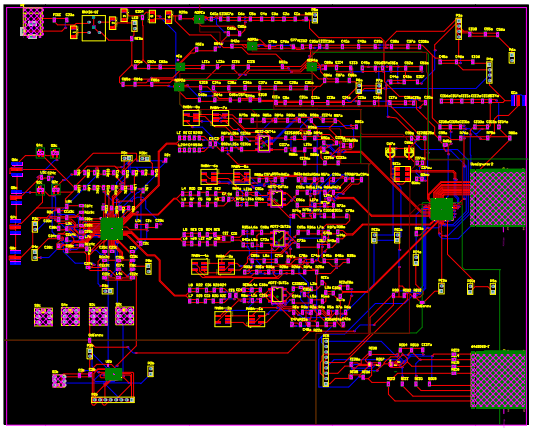

Figure 9 PCB Diagram of System Design

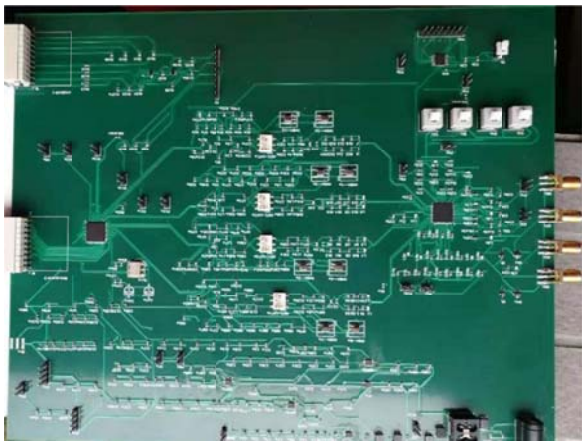

Figure 10 Physical diagram of the system

7. Conclusion

In this paper, a new type of ultrasonic nondestructive testing system is designed. Firstly, the shortcomings of traditional ultrasonic flaw detection system and the new requirements for ultrasonic nondestructive testing in modern testing field are analyzed and discussed. Then, we design a new type of ultrasonic nondestructive testing system to meet the new challenges. The system includes three core functional modules: ultra low noise variable gain amplifier module VGA, precision gain control module and high speed digital to analog conversion module. The high-speed digital-to-analog conversion module is divided into five sub-modules: main control module, analog input module, power supply module, clock module and serial module. Finally, the designed system

is made into a physical board and simulated. The test results show that the new system has many advantages, such as low cost, small size, low power consumption, simple operation and so on. It also lays a solid foundation for the follow-up non-destructive ultrasound imaging system. The research results of this paper can provide technical support and theoretical guidance for ultrasonic nondestructive testing, and have great practical value.

Acknowledgments

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